ABSTRACT OF THE DISCLOSURE

A computer system reads data corresponding to an IC layout target layer and performs an etch simulation on the target layer. Etch biases are calculated and the inverse of the etch biases are used to produce a new target layer. The new target layer is provided as an input to an optical process correction (OPC) loop that corrects the data for image/resist distortions until a simulation indicates that a pattern of objects created on a wafer matches the new target layer. In another embodiment of the invention, original IC layout data is provided to both the OPC loop and an etch simulation. Etch biases calculated by the etch simulation are used in the OPC loop in order to produce mask/reticle data that will be compensated for both optical and resist distortions as well as for etch distortions.